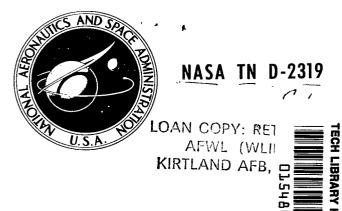
NASA TECHNICAL NOTE



A SOLID STATE SATELLITE SEPARATION SEQUENCE TIMER

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SUMMARY

A solid state satellite separation sequence timer is described which is designed to provide for the payload separation sequence at appropriate intervals. Two methods of firing explosive charges are discussed. The versatility of a solid state system is noted as well as its qualification for adverse environments. Examples of the systems used in the UK-1/S-51 (Ariel I) and UK-2/S-52 satellites are given.

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INTRODUCTION

Important to the success of a satellite is the proper sequence of events between final stage burnout and payload separation. When orbit entry has been achieved, satellite despin operations must be initiated; the various booms, experiments and solar paddles must be extended; and the satellite must be separated from the last stage of the vehicle.

Mechanical timers driven by clocks or motors have traditionally been used for this purpose. But in several instances their reliability has been in question, especially at the extreme vibration levels experienced on launch vehicles. Thus there arises the need for a more reliable timer to perform the timing functions and provide appropriate outputs to fire explosive charges used to initiate events. The timer developed to fill this need is a solid state system using basic timing circuits that are simple in operation and have a flight history of high reliability. Emphasis was placed on a system that lends itself to easy time adjustments for last minute changes or use in other applications. The final design incorporates possibilities for safe redundant tie-ins between parallel systems.

FUNCTIONAL REQUIREMENTS

Typical functions of a satellite separation system are:

- 1. Timer Initiation;
- 2. Deployment of despin mechanism;
- 3. Erection of inertia booms;
- 4. Erection of solar paddles; and
- 5. Payload separation from last stage.

The sequence timers described here are designed to provide outputs anywhere within the following time intervals by means of adjusting a single resistor per interval: The long interval is 0 to 2000 sec; the short interval; 0 to 90 sec.

The design of the separation timer is such that each interval timer is independent and may be connected in series or parallel with any number of other interval timers in any order. Therefore, the order of the intervals and the total number of intervals is dependent only upon the application requirements.

ACCURACY

The accuracy of the timing intervals depends on the degree of compensation used. Off the shelf components with no compensation will yield ± 10 percent or better accuracy over the temperature range of -20° C to $+70^{\circ}$ C. Selection of low-temperature coefficient, low-leakage timing capacitors will yield ± 5 percent in this temperature range. Accuracy of ± 2 percent may be obtained by combinations of bias and timing-current compensation.

POWER REQUIREMENTS

A complete system containing one long-interval timer and three short-interval timers in series, exclusive of the power required to fire the explosive charges, requires approximately 50 mw of power at 12v dc during the timing intervals. Less than 1/4 mw is required before and after the timing interval. The lower limit of operating voltage is 9v as dictated by the decade divider. The upper limit is generally governed by the voltage limit of the capacitors used. In this design 20v capacitors were used at a maximum operating voltage of 18v.

ENVIRONMENTAL LIMITS

The timer operates reliably under the following test conditions:

Temperature: -35° to $+80^{\circ}$ C (at atmos-

pheric pressure)

Thermal

Vacuum: -15° to $+60^{\circ}$ C (at 10^{-6} mm

Hg)

Vibration:

10 to 5000 cps (at maximum

acceleration of 54g).

PRINCIPLES OF OPERATION

Long Interval Timing

A block diagram of the timing circuit used for intervals up to 2000 sec is shown in Figure 1. A start pulse or gate turns on the silicon

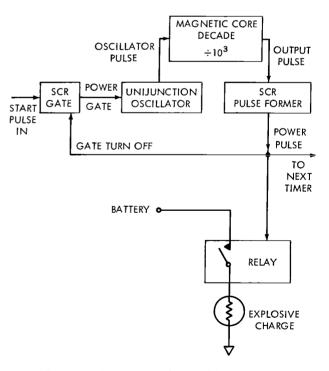


Figure 1—Long interval timer block diagram (0-2000 sec).

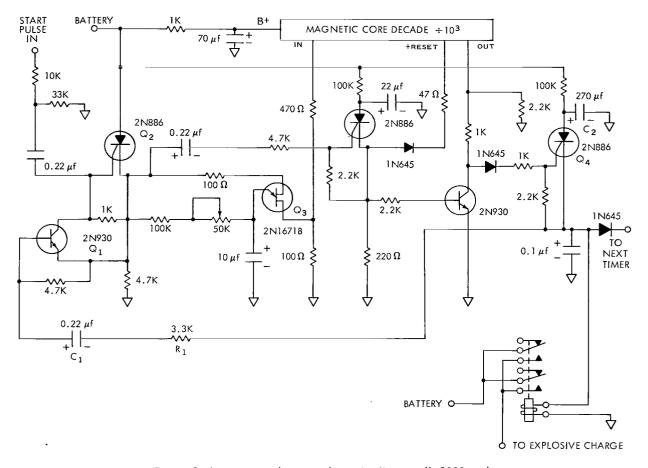


Figure 2—Long interval timer schematic diagram (0-2000 sec).

controlled rectifier (SCR) gate. This connects power to a unijunction-transistor relaxation oscillator. Three incremental magnetic core decade counter-stages are used to provide a pulse-frequency division of 1000 to 1. The output pulse from the counter fires a SCR. The resulting power pulse is used to:

- 1. Operate the firing relay for the explosive charges;
- 2. Start the next timing circuit; and
- 3. Turn off the timing circuit.

Timing turnoff is accomplished as shown in the schematic diagram (Figure 2). The timer output pulse is fed through R_1 and C_1 to the base of Q_1 . This causes Q_1 to conduct, providing connection of gate and cathode of the input SCR (Q_2) , thus removing its drive. Q_2 is therefore turned off, removing power from the unijunction oscillator.

Short Interval Timing

Figure 3 shows a block diagram of the timing circuit used for intervals up to 90 seconds. This diagram is different from the long interval diagram in that a unijunction transistor used as

a one-shot multivibrator replaces the oscillator and counter combination. The time interval is adjusted by choice of the R_1 - C_1 combination in the emitter circuit of the unijunction transistor (Q_3) (Figure 4). The time interval may be safely varied up to 90 sec using a $120\mu f$ wet-slug tantalum capacitor and to 75 sec using a $180\mu f$ tantalum foil capacitor. The difference in the maximum intervals is due to the inherent difference in leakage of the two types of capacitors. The lower leakage of the wet-slug type allows a higher resistance value for R_1 , and thus a longer maximum time interval.

Relay Method of Firing Explosive Charges

The time constant of the power pulse to the relay is determined, at a given system voltage, by capacitor C2 at the anode of the output SCR

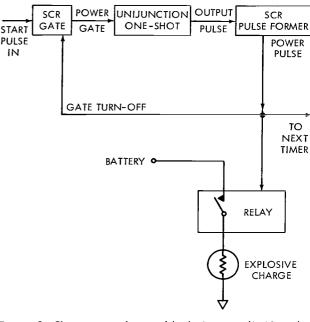


Figure 3—Short interval timer block diagram (0-90 sec).

 ${\bf Q}_4$ (Figures 2 and 4), and the resistance of the relay coil. This time constant is chosen to provide a switch closure of at least 80 msec which is about 10 times the normal firing time of the explosive charge used. The method of firing the explosive charge through a momentary switch closure is chosen to prevent shorting of the system battery in the event the conductive path through the charge should fail to open when it is fired.

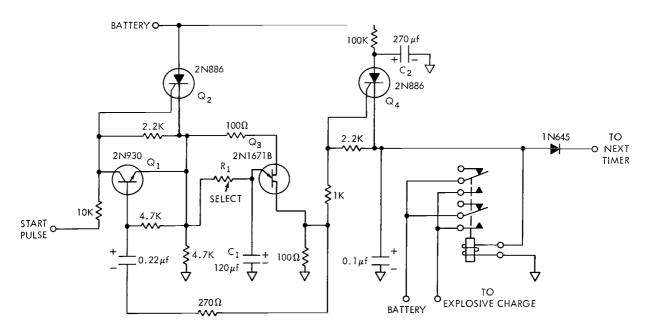


Figure 4—Short interval timer schematic diagram (0-90 sec).

The relays used have a normal contact rating of 2 amps at 28v dc. However, tests conducted during the timer development show them capable of an average of about 20,000 operations at a 10:1 duty cycle at 12v and the 25 amp maximum current expected through the explosive charges.

Solid State Method of Firing Explosive Charges

The explosive charge may also be fired directly through a SCR (Figure 5). The 2N1882 may be fired by another SCR, or it may be fired directly from the unijunction-transistor output pulse. The 2N1882 in turn fires the high cur-

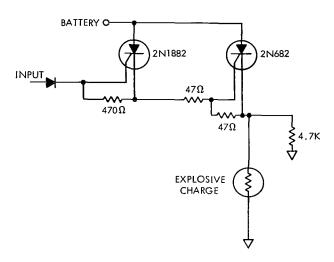


Figure 5—Explosive charge firing circuit.

rent 2N682. The 4.7K resistor to ground prevents the normal transistor leakage current from giving the false indication that the SCR is on at the time the explosive charge is connected. This precaution is required by the normal prelaunch procedure for pyrotechnic installation.

The method of using SCR's has the advantage of keeping the system completely solid state, but cannot be used where the possibility of a shorted explosive charge exists unless some method of current limiting is employed. Current limiting may be achieved by using fuses or low value resistors.

This solid state method was successfully used on the UK-1/S-51 satellite (Ariel I, 1962 ∘2).

Redundancy

Due to the independence of the timing interval and explosive-charge firing circuits, and the fact that the oscillator for each interval is normally off, redundant tie-in may be easily and safely accomplished. This is one of the major advantages of the solid state timer over the often used mechanical timers where time interval error generally cannot be corrected but will accumulate during successive intervals. It is also generally not feasible to provide any redundancy in a mechanical timer except at switch contacts.

Figure 6 shows some possibilities for redundant tie-in between two solid state systems. The line shown as R1 accomplishes initiation of both timers by a single start pulse. Lines R2 and R3 in combination would ensure explosive-charge firing and start pulses to both of the next timing circuits in case of failure of one timing interval. It should be noted that in this type of circuit, the most likely failure mode is an extended interval rather than a shortened interval. Line R4 shows another possibility for ensuring pulses to both explosive-charge firing circuits with outputs from either interval timer. Line R5 would start the following timers in case of failure of either explosive charge firing circuit.

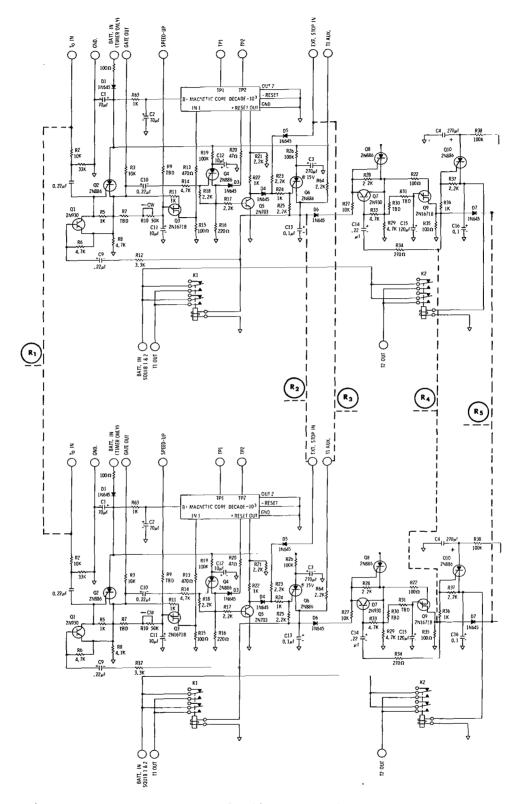


Figure 6-Possible redundant tie-in.

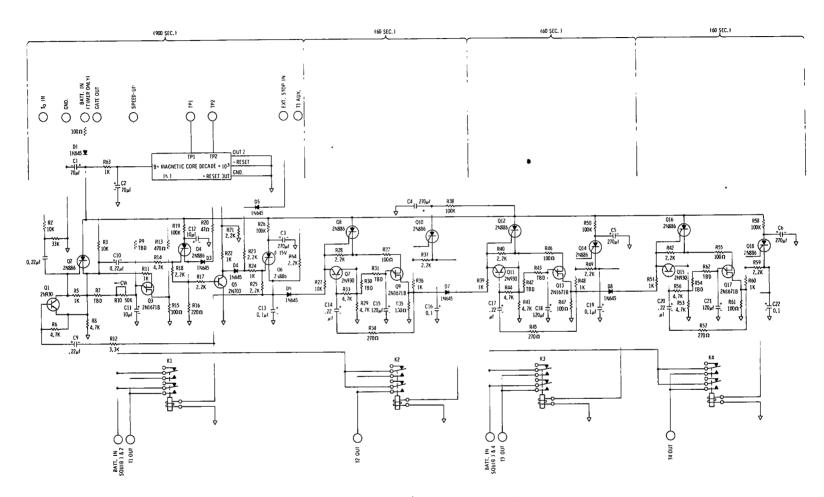


Figure 7—Complete UK-2/S-52 application schematic.

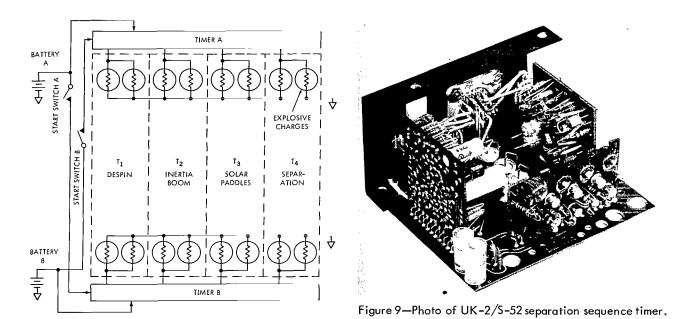


Figure 8-UK-2/S-52 Separation system wiring.

The choice as to what amount of redundancy, if any, is needed can only be decided by considering the particular application and the reliability of the timer initiation mechanism, explosive charges, and associated wiring.

TIMER USE IN UK-2

The complete schematic diagram of the timer used in UK-2/S-52 is shown in Figure 7. In this application, the timer and explosive charges use the same battery. The capacitor C_1 and diode D_1 provide decoupling when the battery voltage drops from a nominal 18v to about 4v at the time of firing each explosive charge.

The wiring of the complete separation system used in UK-2/S-52 is shown in Figure 8. In this application, two sets of batteries, timers, and explosive charges are used. The only tie-in between units is at the explosive charges. No tie-in is made between timers. The UK-2/S-52 timer is shown in Figure 9.

CONCLUSION

The methods developed for timing and explosive-charge firing have been thoroughly tested in the lab and proven in flight. The developed variations on the basic design will allow easy application in future programs. The number of events controlled is merely a matter of adding or deleting identical stages. Needs for various time intervals are met simply by the adjustment of a R-C time constant.

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